



Rodrigues De Oliveira Zanini, P., Rossiter, J., & Homer, M. (2016). Modeling self-priming circuits for dielectric elastomer generators towards optimum voltage boost. In *Electroactive Polymer Actuators and Devices (EAPAD) 2016* (Vol. 9798). (Proceedings of SPIE; Vol. 9798). Society of Photo-Optical Instrumentation Engineers (SPIE). <https://doi.org/10.1117/12.2218650>

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Link to published version (if available):  
[10.1117/12.2218650](https://doi.org/10.1117/12.2218650)

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# Modeling self-priming circuits for dielectric elastomer generators towards optimum voltage boost

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**Abstract.** One of the main challenges for the practical implementation of dielectric elastomer generators (DEGs) is supplying high voltages. To address this issue, systems using self-priming circuits (SPCs) — which exploit the DEG voltage swing to increase its supplied voltage — have been used with success. A self-priming circuit consists of a charge pump implemented in parallel with the DEG circuit. At each energy harvesting cycle, the DEG receives a low voltage input and, through an almost constant charge cycle, generates a high voltage output. SPCs receive the high voltage output at the end of the energy harvesting cycle and supply it back as input for the following cycle, using the DEG as a voltage-multiplier element. Although rules for designing self-priming circuits for dielectric elastomer generators exist, they have been obtained from intuitive observation of simulation results and lack a solid theoretical foundation. Here we report the development of a mathematical model to predict voltage boost using self-priming circuits. The voltage on the DEG attached to the SPC is described as a function of its initial conditions, circuit parameters/layout, and the DEG capacitance. Our mathematical model has been validated on an existing DEG implementation from the literature, and successfully predicts the voltage boost for each cycle. Furthermore, it allows us to understand the conditions for the boost to exist, and obtain the design rules that maximize the voltage boost.

**Keywords:** dielectric elastomer generators, energy harvesting, self-priming circuit, circuit design, dielectric elastomers.

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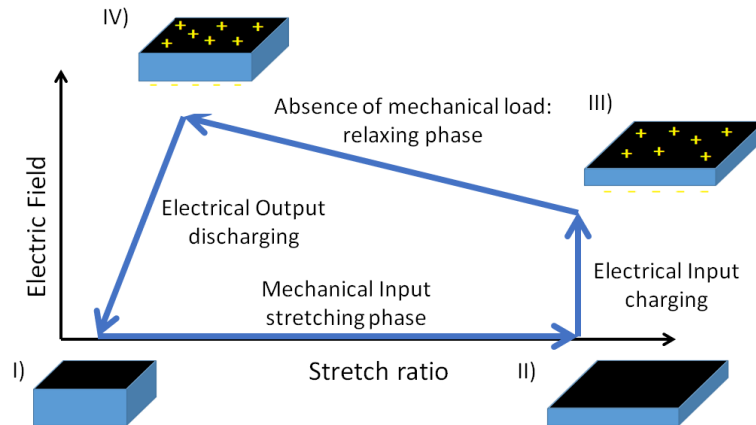
## 1 Introduction

According to the World Energy Council,<sup>1</sup> 1.2 billion people do not have access to electricity. Energy price volatility and greenhouse gas emissions issue accentuate this issue, and point to the need for cheap, reliable and renewable energies. As a new and emerging eletromechanical energy conversion technology, Dielectric Elastomer Generators (DEGs) are one possible solution. With low frequency and wide bandwidth,<sup>2</sup> energy harvesting DEGs have already been reported for use in wave energy generation,<sup>3</sup> human motion energy harvesting<sup>4</sup> and even as thermal machines.<sup>2</sup>

DEGs harvest energy through capacitance change induced by deformation. The energy harvesting happens in cycles; one example with four stages I–IV is illustrated in Figure 1. The transitions between

states in this cycle are as follows.

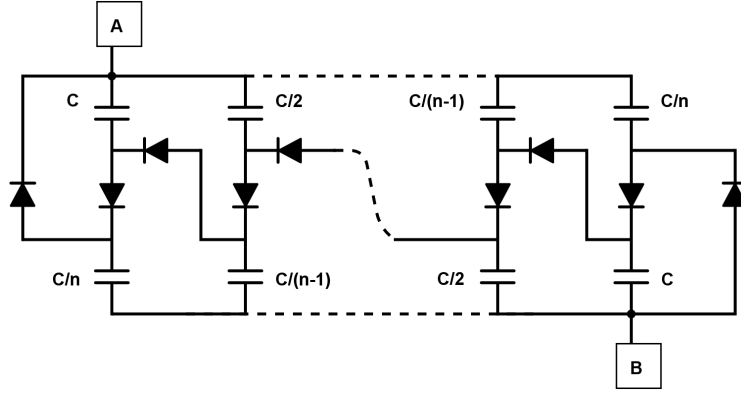
- I→II: From an initially relaxed phase, the DEG is stretched by a mechanical load and increases its capacitance.
- II→III: Once stretched, the DEG is polarized through an electrical energy input.
- III→IV: From stretched and polarized, in an open circuit configuration, the mechanical load is released letting the material relax, so reducing the DEG's capacitance. As the capacitance reduces and the charge stored is maintained constant, there is a voltage rise.
- IV→I: Finally, the DEG is discharged from its more energetic state, back to its initial state.



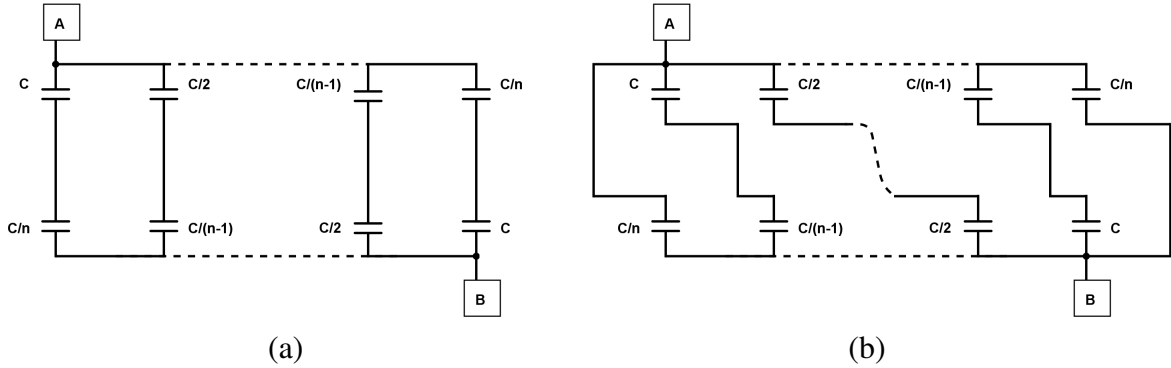
**Fig 1** DEG energy harvesting cycle using relaxation with constant charge

Among the drawbacks of current DEG technology is the necessary condition of inputting electrical energy to polarize the material. Furthermore, the energy output between states IV and I is proportional to the amount of electrical energy used to polarize the DEG between states II and III,<sup>5</sup> so, in order to explore the energy harvesting capabilities at its maximum, one might want to input high voltages.

A solution for generating the high voltage in DEGs is the use of Self-priming Circuits (SPCs), proposed by McKay *et al.*<sup>6</sup> An SPC consists of an inverse charge pump, toggling between high and low capacitance states, depending on its polarization. The circuit is composed of diodes and capacitors, as illustrated in Figure 2. An SPC can be polarized in a High Voltage (HV) form, which has a lower capacitance and will only allow current to charge the capacitors, or in a High Charge (HC) state, which has higher capacitance and will only allow current to flow from the SPC (considering their poles are connected such that  $V_A > V_B$ ).



**Fig 2** SPC general scheme. Adapted from McKay *et al.*<sup>7</sup>



**Fig 3** SPC effective configuration with (a) HV polarization, and (b) HC polarization. Adapted from McKay *et al.*<sup>7</sup>

The advantage of using an SPC is that it allows part of the energy output in a DEG cycle to be stored and used as an input in the following one. Through the use of an SPC it is possible to initially prime the DEG-SPC system with low voltage and, by cycles of stretching-relaxing the DEG, bring the system to high voltage and increase its energy output.

SPCs have been a promising topic of research, and upgrades have been made to their layout (see Figure 2), such as using antagonistic DEG membranes to replace the capacitors normally used,<sup>8</sup> or the use of Dielectric Elastomer Switches (DES), which are flexible resistive elements incorporated in the membrane that are able to toggle between high and low resistance, and replace the diodes in the SPC.<sup>9</sup>

Here, we report a mathematical model of the simple SPC-DEG system and, through it, provide general design rules. Although design rules have already been suggested,<sup>7</sup> they appear to have been based on intuitive observation of numerical simulation results. We will derive analytic expressions for the rules, and demonstrate why they work and how they can be improved, with the overall aim of better understanding the SPC as a voltage-boosting element that can solve the high-energy input issue in DEG cycles.

## **2 Self-priming circuits**

As described previously for the DEG energy harvesting cycle, the DEG-SPC system also passes through different phases during the DEG stretch-relax cycle. These cycle phases and the model assumptions are detailed below; the resulting voltage and capacitance are shown in Figure 4.

## 2.1 Cycle phases

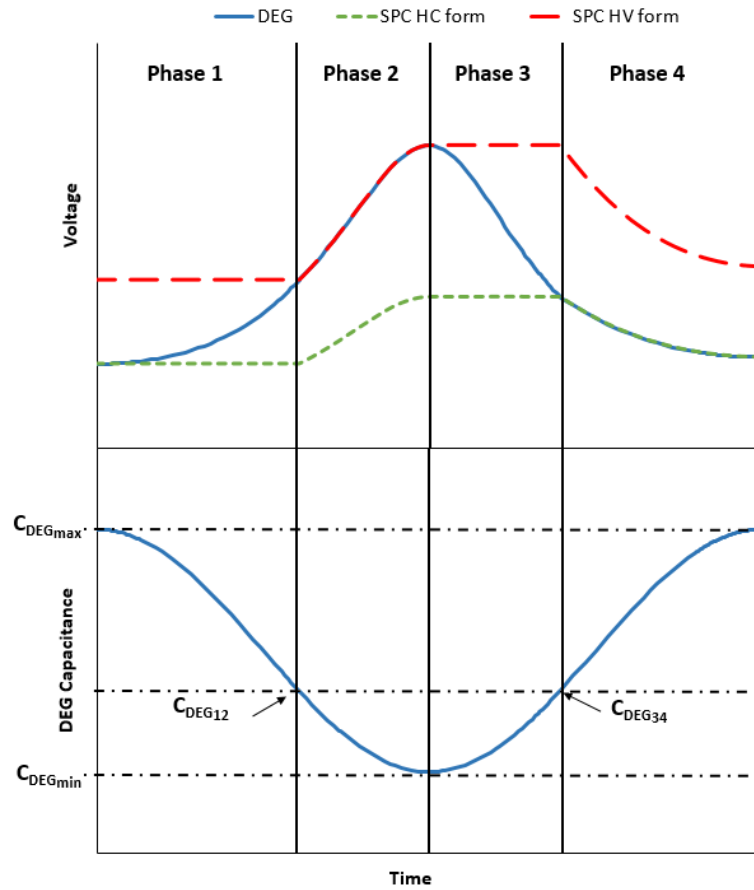
Using an SPC connected in parallel with the DEG, we can increase the voltage every time the DEG is cycled. Note that the voltages represented in Figure 4 for the HV and HC forms reflect the voltage if the SPC was simply a capacitor with constant capacitance with a certain amount of charge stored. However, given the arrangement of the diodes, charge only flows into the SPC in its HV form and from it in its HC form. If we consider a DEG stretch-relax cycle between fixed maximum and minimum stretch, we can describe the DEG-SPC cycle in four phases (see Figure 5).

**Phase 1** Starting from a point similar to stage III described in Figure 1, the DEG capacitance starts decreasing as it relaxes. Given that its voltage is not yet higher than that on the SPC in HV form, charge will not flow to the SPC. Similarly, the DEG voltage is higher than the SPC voltage in its HC form, thus, there is no charge flow from the SPC into the DEG. Consequently, we have a voltage increase in the DEG (similar to the process III→IV).

**Phase 2** As the voltage on the DEG achieves the same level of that in the SPC in its HV form, the DEG starts discharging into the SPC. The DEG voltage keeps rising due to the capacitance decrease, and the SPC voltage rises due to its charging.

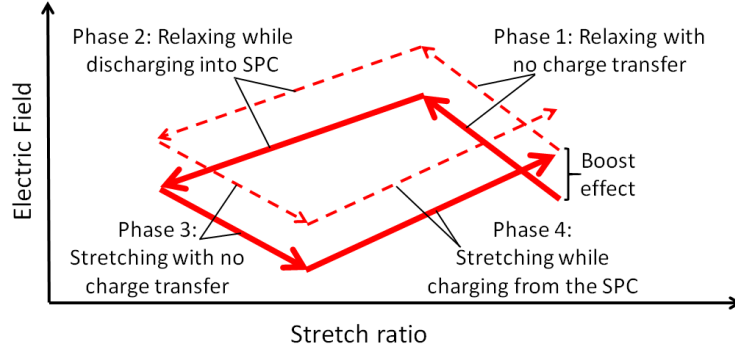
**Phase 3** Once the DEG stops relaxing and starts being stretched again, its capacitance starts to rise. As a consequence, the voltage starts dropping in the DEG. In an similar situation to Phase 1, there is no charge flow between the SPC and the DEG, as the first has a higher voltage in its HV form and a lower voltage in its HC form, preventing the flow of charge to or from the SPC.

**Phase 4** When the voltage in the DEG reaches that of the SPC in its HC form, a charging current starts to flow from the SPC. As the DEG has a capacitance decrease, its voltage keeps dropping. The SPC also loses charge due to drain into the DEG. At the moment the DEG's capacitance stops rising and starts decreasing again, the cycle restarts, going back to Phase 1.

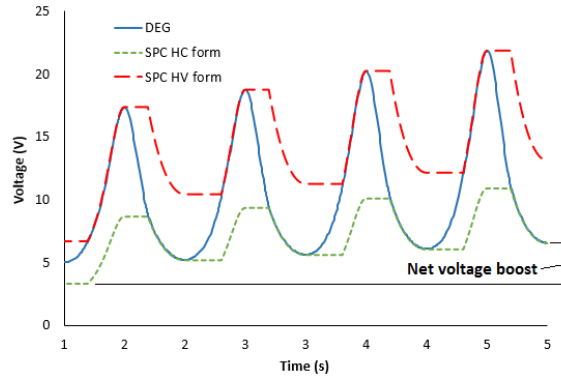


**Fig 4** The four phases of the cycle.

We can see how the cycle produces an overall system voltage boost in Figure 6, which illustrates the boosting process, showing the DEG-SPC voltage and the voltage in the SPC given by its stored charge and the capacitance on each of its forms.



**Fig 5** The DEG-SPC cycle, shown as electric field as a function of stretch.



**Fig 6** Voltage as a function of time for the DEG and the SPC, in both its HC and HV form.

## 2.2 SPC model considerations

In the HV form of the SPC there are  $n$  branches in parallel, each with capacitance  $C/(n+1)$ , and, in the HC form, there are  $n+1$  stages with capacitance  $C/n$ . Thus, the equivalent capacitance of the circuit can be written in each form as:

$$C_{\text{SPCHV}} = C \left( \frac{n}{n+1} \right), \quad (1)$$

$$C_{\text{SPCHC}} = C \left( \frac{n+1}{n} \right). \quad (2)$$



Considering the initial situation when the circuit is primed with a voltage  $V_0$ , in an equilibrium condition (no current flow), we can calculate that each capacitor with capacitance  $C$  has a voltage drop of

$$V_{C_0} = \frac{2V_0}{(2n+1)}. \quad (3)$$

This implies that the initial voltage in which the HV form will be active is

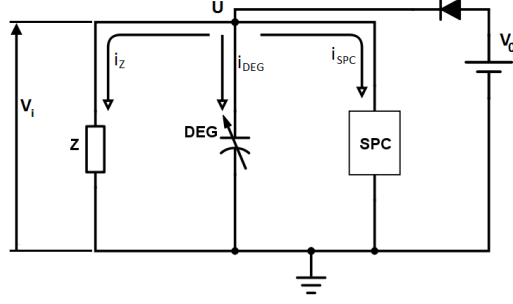
$$V_{\text{SPCHV}} = (n+1)V_{C_0}. \quad (4)$$

The same reasoning can be applied to the HC form; the voltage at which it will be triggered is

$$V_{\text{SPCHC}} = \frac{n}{n+1}V_{\text{SPCHV}}. \quad (5)$$

### 3 Modeling the boost cycle phases

In this section we introduce a general model of each phase of the DEG-SPC voltage boosting cycle. Figure 7 illustrates the high-level circuit scheme of the DEG-SPC system, attached to a load. The source  $V_0$  is used only to supply an initial priming for the DEG-SPC system and the diode prevents charge to flow back through it when the voltage boost occurs. For this model, we consider that the DEG stretches and relaxes sinusoidally between two fixed positions, creating maximum and minimum area configurations, thus corresponding to a simple variable capacitor oscillating sinusoidally between  $C_{\text{DEG}_{\min}}$  and  $C_{\text{DEG}_{\max}}$ .



**Fig 7** Electronic circuit scheme of DEG-SPC system attached to a load.

### 3.1 Phase 1

We consider the cycle starting from an initially charged state (provided by the source,  $V_0$ ) and with the DEG relaxing from a stretched position that produces capacitance  $C_{\text{DEG}_0}$ .

As explained previously, while the DEG relaxes, its capacitance is reduced and the voltage increases. No charge exchange happens between the SPC and the DEG, since the voltage is not large enough to trigger the HV form of the SPC. Meanwhile, some of the charge leaks through the load (which represents either an energy harvesting impedance or simple losses/leakage in the system), resulting in

$$Q(t) = Q_0 - \frac{V(t)}{Z} = V_0 C_{\text{DEG}_0} - \frac{V(t)}{Z}, \quad (6)$$

where  $Q(t)$  is the charge in the DEG and  $Q_0$  is the charge level in the DEG provided by the voltage source  $V_0$ . The voltage in Phase 1,  $V_1$ , will then vary with time as

$$V_1(t) = V_0 \left( \frac{C_{\text{DEG}_0}}{C_{\text{DEG}}(t) + t/Z} \right). \quad (7)$$

As the voltage increases, it reaches the level held by the SPC in its high voltage form,  $V_{\text{SPCHV}}$ . At this point we transition to the next phase, in which the DEG starts discharging into the SPC. The DEG state in which the transition occurs at a time  $t_{12}$ , which can be found as the first solution of  $V_1(t_{12}) = V_{\text{SPCHV}}$ . From Equation 7 this is equivalent to

$$V_{\text{SPCHV}} = V_0 \left( \frac{C_{\text{DEG}_0}}{C_{\text{DEG}}(t_{12}) + t_{12}/Z} \right). \quad (8)$$

### 3.1.1 Phase 2

During Phase 2, the DEG voltage increases and not only supplies current to the load but also discharges into the SPC in its HV form. To describe the voltage behavior, we start by writing Kirchhoff's current law for the node U (see Figure 7) in a general case:

$$\frac{V(t)}{Z} + C_{\text{SPC}} \frac{dV(t)}{dt} + C_{\text{DEG}}(t) \frac{dV(t)}{dt} + V(t) \frac{dC_{\text{DEG}}(t)}{dt} = 0. \quad (9)$$

Given that  $C_{\text{SPC}} = C_{\text{SPCHV}}$  in this phase, and considering the initial conditions of this phase  $C_{\text{DEG}}(t_{12}) = C_{\text{DEG}_{12}}$  and  $V(t_{12}) = V_{\text{SPCHV}}$ , Equation 9 can be solved to give us the voltage in Phase 2,  $V_2(t)$ , as

$$V_2(t) = V_{\text{SPCHV}} \left( \frac{C_{\text{SPCHV}} + C_{\text{DEG}_{12}}}{C_{\text{SPCHV}} + C_{\text{DEG}}(t)} \right) e^{\beta_2(t)}, \quad (10)$$

where

$$\frac{d\beta_2}{dt} = -\frac{1}{Z(C_{\text{SPCHV}} + C_{\text{DEG}}(t))}. \quad (11)$$

The peak voltage can then be found when the DEG capacitance reaches its minimum value, by using  $C_{\text{DEG}}(t_{23}) = C_{\text{DEG}_{\min}}$ , noting that  $t_{23}$  marks the transition time to Phase 3.

### 3.2 Phase 3

After reaching its maximum voltage, the DEG starts being stretched again and its capacitance increases, leading to a voltage drop. The current through the SPC ceases, since its voltage in the HC form is higher than that of the DEG. Thus, there is only current from the DEG to the attached load, as in Phase 1. Now, the voltage drops from the peak voltage,  $V_{\max}$  achieved when the DEG reaches its minimal capacitance,  $C_{\text{DEG}_{\min}}$ . Using the same approach as before, we obtain

$$V_3(t) = V_{\max} \left( \frac{C_{\text{DEG}_{\min}}}{C_{\text{DEG}}(t) + t/Z} \right). \quad (12)$$

As the voltage drops, it will reach the potential of the SPC in its HC state,  $V_{\text{SPC}_{\text{HC}}}$ , at time  $t = t_{34}$ , and, at this point, we have a transition to the next phase. We can find the DEG state based on its capacitance when the DEG will start charging up using the energy stored in the SPC,  $C_{\text{DEG}_{34}} = C_{\text{DEG}}(t_{34})$ . Substituting into Equation 12, we have

$$V_{\text{SPC}_{\text{HC}}} = V_{\max} \left( \frac{C_{\text{DEG}_{\min}}}{C_{\text{DEG}_{34}} + t_{34}/Z} \right). \quad (13)$$

### 3.3 Phase 4

During Phase 4, the DEG voltage reaches the SPC voltage in its HC form and starts charging up from it. As this phase uses the same circuit analyzed in Phase 2, we use again the generalized Equation

9 as a starting point. We apply the initial conditions for the phase transition at  $t_{34}$ , and obtain that

$$V_4(t) = V_{\text{SPC}_{\text{HC}}} \left( \frac{C_{\text{SPC}_{\text{HC}}} + C_{\text{DEG}_{34}}}{C_{\text{SPC}_{\text{HC}}} + C_{\text{DEG}}(t)} \right) e^{\beta_4(t)}, \quad (14)$$

with

$$\frac{d\beta_4}{dt} = -\frac{1}{Z(C_{\text{SPC}_{\text{HC}}} + C_{\text{DEG}}(t))}. \quad (15)$$

### 3.4 Following cycle

From Equation 14, we can see clearly that a local minimum will be obtained using the maximum value of  $C_{\text{DEG}}(t)$ . As the voltage curve reaches this local minimum, we return to phase 1 of the cycle, but this time using the DEG's maximum capacitance and the minimum voltage from the previous cycle as initial conditions.

## 4 Modeling voltage boost

Given the model described above, we study a case focused on boosting the voltage, without concerns regarding energy output through external loads and neglecting the effects of non ideal elements. Thus, we obtain a simplified version of the model by neglecting the attached impedance,  $Z$ , considering it infinite and ignoring the current drained through it.

### 4.1 Simplified model

Through Equations 7, 10, 12 and 14 we have described the DEG-SPC system cycle considering current drained through a load with impedance  $Z$ . If we consider  $Z \rightarrow \infty$  and that it is not the first cycle to run, we can define the voltage behavior as a new function,  $V^*(t)$ , which is given in each of

the phases described previously by:

$$V_1^*(t) = V_{\min} \left( \frac{C_{\text{DEG}_{\max}}}{C_{\text{DEG}}(t)} \right), \quad (16)$$

$$V_2^*(t) = V_{\text{SPC}_{\text{HV}}} \left( \frac{C_{\text{SPC}_{\text{HV}}} + C_{\text{DEG}_{12}}}{C_{\text{SPC}_{\text{HV}}} + C_{\text{DEG}}(t)} \right), \quad (17)$$

$$V_3^*(t) = V_{\max} \left( \frac{C_{\text{DEG}_{\min}}}{C_{\text{DEG}}(t)} \right), \quad (18)$$

$$V_4^*(t) = V_{\text{SPC}_{\text{HC}}} \left( \frac{C_{\text{SPC}_{\text{HC}}} + C_{\text{DEG}_{34}}}{C_{\text{SPC}_{\text{HC}}} + C_{\text{DEG}}(t)} \right), \quad (19)$$

where  $V_{\min}$  corresponds to the local minimum in the DEG voltage curve achieved at the end of Phase 4 and  $V_{\max}$  the local maximum voltage obtained at the end of Phase 2.

Following the same approaching and neglecting the current through the impedance, we can also describe the capacitances in the DEG at the transition between phases:

$$C_{\text{DEG}_{12}} = \frac{V_{\min} C_{\text{DEG}_{\max}}}{V_{\text{SPC}_{\text{HV}}}}, \quad (20)$$

$$C_{\text{DEG}_{34}} = \frac{V_{\max} C_{\text{DEG}_{\min}}}{V_{\text{SPC}_{\text{HC}}}}, \quad (21)$$

where, in this scenario,

$$V_{\text{SPC}_{\text{HV}}} = \frac{n+1}{n} V_{\min} \quad (22)$$

$$V_{\text{SPC}_{\text{HC}}} = \frac{n}{n+1} V_{\max}. \quad (23)$$

## 4.2 Voltage boost model

We say that there has been a voltage boost if the peak voltage in a cycle is higher than the peak in the previous one. We evaluate the boost through the parameter  $B$ , defined as the ratio between a maximum voltage in a cycle and that of the previous one. The set of equations described in Section 4.1 allows us to determine the relation between a local maximum in the voltage curve for a cycle,  $V_{\max_j}$  and the process can be extended to the next local maximum,  $V_{\max_{j+1}}$ , located in the following cycle. The equation can be broken down using the basic parameters  $C$  and  $n$ , which reflect the SPC design, and the DEG capacitance swing between minimum capacitance,  $C_{\text{DEG}_{\min}}$ , and maximum capacitance,  $C_{\text{DEG}_{\max}}$ , yielding

$$B = \frac{V_{\max_{j+1}}}{V_{\max_j}} = \frac{C^2 + (C_{\text{DEG}_{\min}} + C_{\text{DEG}_{\max}})C + C_{\text{DEG}_{\min}}C_{\text{DEG}_{\max}}}{C^2 + \left( \frac{n^2 C_{\text{DEG}_{\max}} + (n+1)^2 C_{\text{DEG}_{\min}}}{n(n+1)} \right) C + C_{\text{DEG}_{\min}}C_{\text{DEG}_{\max}}}. \quad (24)$$

Equation 24 provides insights about several aspects of system design and behavior. First, it allows us to verify the minimum requirements for boost to exist, when  $B > 1$ . It can also be seen that the ratio between maximum voltage in a cycle and that of the previous one stays constant if both the SPC characteristics, and the DEG capacitance swing, are maintained. Another possibility is verifying the design parameters that lead to a maximum boost, which can be achieved easily by differentiation. We can search for the value of  $C$  that maximizes the boost and also determine how increasing the number of stages,  $n$ , affects the SPC.

#### 4.2.1 Condition for boost to exist

To obtain boost, we must have  $B > 1$ , which leads us straightforwardly to the condition

$$n > \frac{1}{C_{\text{DEG}_{\text{max}}}/C_{\text{DEG}_{\text{min}}} - 1}. \quad (25)$$

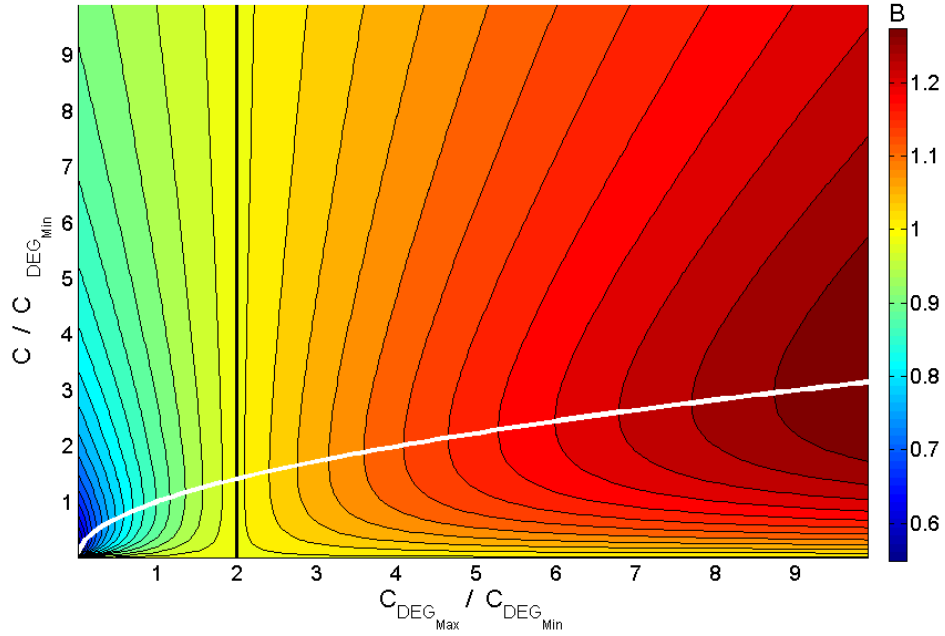
#### 4.2.2 Maximum boost

In order to choose the value of  $C$  which will provide the maximum boost,  $B$ , we seek solutions of  $dB/dC = 0$ , which gives

$$C = \sqrt{C_{\text{DEG}_{\text{min}}} C_{\text{DEG}_{\text{max}}}}. \quad (26)$$

We can see in Figure 8 the importance of selecting the right value of  $C$ , as the voltage could even decrease at each cycle if inappropriately chosen. If the capacitance of the SPC is too high, the capacitance swing from the DEG would be negligible when compared to the SPC's capacitance; the Phase 2 voltage rise would stop as all the charges would flow from the DEG to the SPC instead of increasing the voltage. On the other hand, if the SPC capacitance is too low, it would not be able to accommodate enough charge to keep the boosting process going. In this case, we would have a voltage swing due exclusively to a DEG capacitance change when it holds constant charge, having only Phases 1 and 3 of the cycle (Equations 17 and 19 would converge to Equations 16 and 18). It is also possible to verify how relevant the capacitance change, evaluate hered as  $C_{\text{DEG}_{\text{max}}}/C_{\text{DEG}_{\text{min}}}$  is, as its effect on the voltage boost is clearly visible in Figure 8. The higher the capacitance change, the higher the maximum voltage boost possible.





**Fig 8** Voltage boost,  $B$ , shown as a function of DEG capacitance change,  $C_{\text{DEG}_{\text{max}}}/C_{\text{DEG}_{\text{min}}}$ , for different SPC base capacitance,  $C$ , for a one stage SPC ( $n = 1$ ). The white line indicates the peak boost as suggested by Equation 26. The thick black line corresponds to  $B = 1$  and separates the region with boost (right) from that where the condition in Equation 25 is not fulfilled and  $B < 1$  (left)

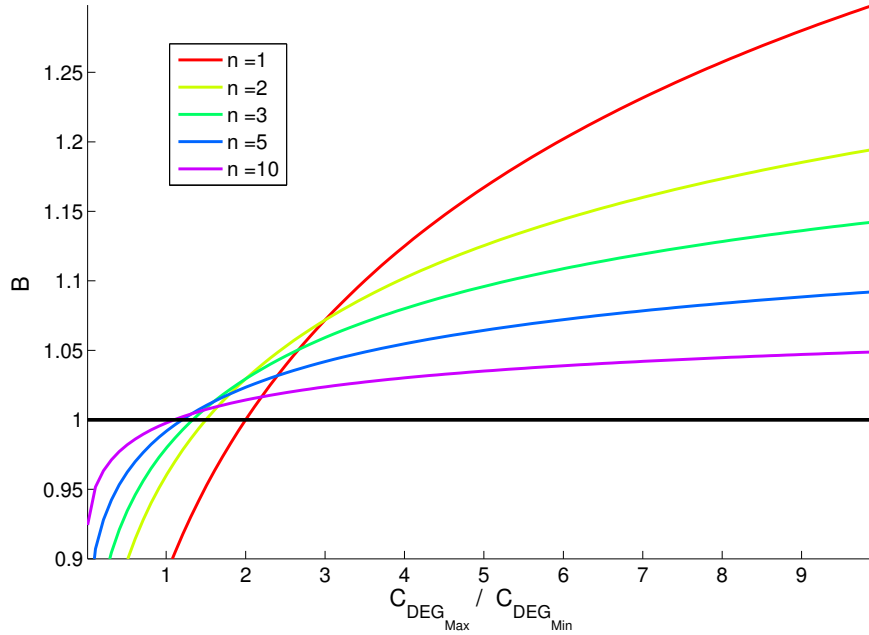
#### 4.2.3 Effect of the number of stages

The number of stages will influence the denominator of Equation 24, specifically the coefficient  $A$  of the linear term in  $C$ ,

$$A = \frac{n^2 C_{\text{DEG}_{\text{max}}} + (n+1)^2 C_{\text{DEG}_{\text{min}}}}{n(n+1)}. \quad (27)$$

It is trivial to observe that if  $n \rightarrow \infty$ ,  $A \rightarrow C_{\text{DEG}_{\text{max}}} + C_{\text{DEG}_{\text{min}}}$ , hence, the denominator of Equation 24 becomes the same as the numerator and there is no boost. We can find the number of stages that maximises the boost by solving  $dB/dn = 0$  for  $n$ , and comparing the values of  $B$  for the two integers either side of the turning point. We can also verify that the maximum boost is obtained for  $n = 1$  if  $C_{\text{DEG}_{\text{max}}}/C_{\text{DEG}_{\text{min}}} > 3$ . On the other hand, Figure 9 illustrates how increasing the number

of stages allows the boost to exist in a broader range of situations, when the capacitance swing is reduced, though it also shows a reduction in the voltage boost. This can be explained by the decrease in the difference of the SPC capacitance when toggled between its HV and HC forms, decreasing its effectiveness. Looking back at Equations 1 and 2, the more stages are used, the closer the SPC effect becomes of that of a simple capacitor with capacitance  $C$ .

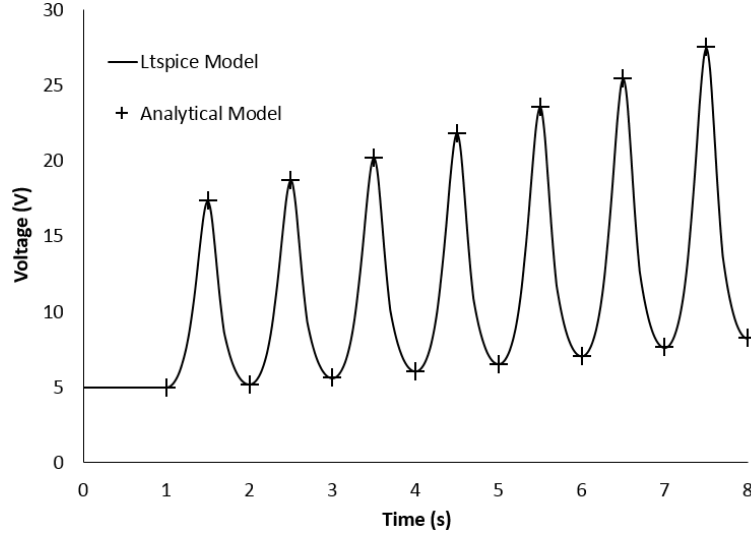


**Fig 9** Voltage boost,  $B$ , versus the DEG's capacitance swing,  $C_{\text{DEG\_max}}/C_{\text{DEG\_min}}$ , for different numbers of stages,  $n$ . The black line corresponds to  $B = 1$ , and separates the region with boost (above) from that without (below).

## 5 Model validation

In order to validate the model, we compared its results with those obtained through the already validated model by McKay in LT Spice.<sup>10</sup> The model was built with a one-stage SPC ( $n = 1$ ) using capacitors of 1 nF. The DEG's capacitance oscillated in a cycle between 2 nF and 8 nF. The circuit was initially primed at 5 V. Only ideal elements were used and no load was considered (both for the

present model and in the circuit). Figure 10 shows that the model agrees very well with the LT Spice simulation with errors of less than 0.5%.



**Fig 10** Comparison of the voltage curve for LT Spice model (black line) and the maximum/minimum values obtained through the analytical method (crosses).

Another important point that validates the current analysis is the correspondence with the rules proposed in McKay *et al.*<sup>7</sup> There, it was suggested that  $C$  and  $n$  should be chosen such that

$$C_{SPCHC} = C_{DEG_{\max}}, \quad (28)$$

and

$$\frac{(n+1)}{n} = \sqrt{\frac{C_{DEG_{\max}}}{C_{DEG_{\min}}}}. \quad (29)$$

Uniting both of these conditions, we get to the same choice of  $C$  expressed in Equation 26. In addition,  $n$  is chosen in a way that will necessarily obey the condition expressed in Equation 25. In contrast, using Equation 26 and observing the condition in Equation 25, we are able to choose the parameters

$C$  and  $n$  independently.

## 6 Conclusion

We have developed an analytical model that describes the physics behind each phase of the cycle of a DEG-SPC system with a load attached to it. Based on this model, we obtained a simplified version, from which we derived a simple closed-form analytic expression that describes the boost per cycle of the DEG-SPC system. From this, we derived the condition for the boost to exist, the ideal parameters for the SPC, and also demonstrated how their variation affects the final voltage boost. In addition, we validated the simplified model by comparing it with another previously validated model<sup>10</sup> showing very good agreement. We have also provided a theoretical basis for the understanding of the SPC design rules previously proposed.<sup>7</sup>

## Acknowledgments

Zanini was supported by the Science without Borders scheme from the National Council for Scientific and Technological Development (CNPq) of the Brazilian Government. Rossiter was supported by UK Engineering and Physical Sciences Research Council (EPSRC) Research Grant EP/M020460/1.

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